WHAT WE CLAIM ARE:

1. A method of manufacturing a semiconductor device comprising the steps of:

(a) evacuating a sputtering chamber to a pressure of 1.5×10^{-8} torr to 9×10^{-8} torr and heating a silicon substrate to a temperature of 330 °C to 395 °C;

(b) sputtering Co on said heated silicon substrate;

(c) after said step (b), forming a cap layer having a small oxygen transmission performance on said silicon substrate without exposing said silicon substrate in air;

(d) after said step (c), performing primary annealing;

(e) after said step (d), removing said cap layer and unreacted Co; and

(f) after said step (e), performing secondary annealing by heating said silicon substrate to a temperature of 450 °C to 750 °C.

2. A method of manufacturing a semiconductor device according to claim 1, wherein said step (a) evacuates said sputtering chamber to a pressure of 1.5×10^{-8} torr to 6×10^{-8} torr.

3. A method of manufacturing a semiconductor device according to claim 1, wherein said step (a) heats said silicon substrate to a temperature of 345 °C to 390 °C.

4. A method of manufacturing a semiconductor device according to claim 1, wherein said step (b) is executed under a condition that a Co film having a

thickness of about 7 nm or thinner is deposited on an insulating film.

5. A method of manufacturing a semiconductor device according to claim 1, wherein said step (b) forms only a Co-Si composite layer on a silicon surface without forming a Co film.

6. A method of manufacturing a semiconductor device according to claim 1, wherein said cap layer is made of a Ti layer or a TiN layer.

7. A method of manufacturing a semiconductor device according to claim 1, wherein said step (c) is executed in a state that a temperature of said silicon substrate is 200 °C or lower.

8. A method of manufacturing a semiconductor device according to claim 1, wherein said step (d) is executed by heating said silicon substrate to a temperature of 450 °C to 550 °C.

9. A method of manufacturing a semiconductor device according to claim 1, wherein said step (f) is executed by heating said silicon substrate to a temperature of 500 °C to 700 °C.

10. A method of manufacturing a semiconductor device according to claim 1, further comprising, before said step (a) a step of:

(x) forming a polysilicon gate electrode, insulating side wall spacers and source/drain regions respectively of a MOS transistor on said silicon

substrate, wherein said steps (a) to (f) form a Co silicide layer on said gate electrode and said source/drain regions by a salicide process.

11. A method of manufacturing a semiconductor device according to claim 1, wherein said step (a) evacuates said sputtering chamber to a pressure of 1.5 x 10^{-8} torr to 6 x 10^{-8} torr and heats said silicon substrate to a temperature of 345 °C to 390 °C.

12. A method of manufacturing a semiconductor device according to claim 1, wherein said step (b) is executed under a condition that a Co film having a thickness of about 7 nm or thinner is deposited on an insulating film and forms only a Co-Si composite layer on a silicon surface without forming a Co film.

13. A method of manufacturing a semiconductor device according to claim 1, wherein said step (a) heats said silicon substrate to a temperature of 345 °C to 390 °C and said step (d) is executed by heating said silicon substrate to a temperature of 450 °C to 550 °C.

14. A method of manufacturing a semiconductor device according to claim 13, wherein said step (f) is executed by heating said silicon substrate to a temperature of 500 °C to 700 °C.

15. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a polysilicon gate electrode, insulating side wall spacers

and source/drain regions respectively of a MOS transistor on a silicon substrate,

(b) evacuating a sputtering chamber to a pressure of 1.5×10^{-8} torr to 9×10^{-8} torr and heating said silicon substrate to a temperature of 330 °C to 395 °C;

(c) sputtering Co on said heated silicon substrate;

(d) after said step (c), forming a cap layer having a small oxygen transmission performance on said silicon substrate without exposing said silicon substrate in air;

(e) after said step (d), performing primary annealing;

(f) after said step (e), removing said cap layer and unreacted Co; and

(g) after said step (f), performing secondary annealing by heating said silicon substrate to a temperature of 450 °C to 750 °C,

wherein said steps (b) to (g) form a Co silicide layer on said gate electrode and said source/drain regions by a salicide process.